International Journal of Nanomedicine

Dovepress
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ORIGINAL RESEARCH

A newly developed transparent and flexible one-transistor memory device using advanced nanomaterials for medical and artificial intelligence applications

This article was published in the following Dove Press journal:
International Journal of Nanomedicine

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Background: Artificial intelligence (AI) integrated circuits (IC) have memory devices as the key component. Due to more complex algorithms and architectures required by neuroscience and other medical applications, various memory structures have been widely proposed and investigated by involving nanomaterials, such as memristors.

Methods: Due to reliability issues of mass production, the dominant memory devices in many computers are still dynamic random access memory (DRAM). A DRAM has one transistor and one capacitor, and so it contains two devices and requires a more compact design to replace.

Results: A one-transistor memory device which is more compact than DRAM is proposed. As far as the authors know, this is the first/novel flexible and transparent one-transistor memory device without any additional process to make a typical transistor and which is based on polyvinyl alcohol. By using indium-titanium-oxide (ITO) as the metal gate, PVA as the dielectric layer and In-Ga-Zn-O (IGZO) as the channel, the memory is implemented mainly based on amorphous oxides and transparent flexible nanomaterials. The charge storage for the memory function was investigated here and is attributed to the mechanism of charge trapping between the ITO/IGZO junctions. It shows typical artificial synaptic transmission behaviors such as EPSC (excitatory postsynaptic currents).

Conclusion: Such a first flexible and transparent one-transistor memory device based on PVA has one capacitor less than DRAM and could be a potential and promising candidate as an alternative for DRAM, especially in the highly complex AI chips needed for numerous medical applications. The flexible memory nanodevice based on flexible dielectrics such as PVA, which shows typical memory and artificial synaptic behaviors, could also be suitable for portable, flexible, transparent or skin-like medical applications.

Keywords: flexible, transparent, one-transistor memory, micro-nano electronics, artificial intelligence

Introduction

The neuromorphic computing paradigm uses memory devices as a key component.[1–3] As the most fundamental component in integrated circuits (IC), memory devices have been widely investigated with numerous updated designs.[4–21] Memristors have attracted much attention due to their applications, such as multi-levels and potentials in AI circuits.[7] Semi-floating gate memory has been proposed based on 2D

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materials.[9] ReRAM, STT-MRAM and PRAM were also proposed due to some special characteristics including fast speed.[1] Nanodevices have been studied also.[15] However, these all still encounter reliability issues in mass production and application, and may require advanced nanomaterials or high technology different from the dominant silicon-based technology. For instance, organic memory requires organic materials,[3] and a transistor with a semi-floating gate requires 2D materials and additional steps for the semi-floating gate.[6] Electrical properties of a memristor are mainly controlled by 2-terminal technology, which is more difficult to control than those of the transistor with mature 3- or 4-terminal technology and high reliability.[4] Hence, their applications in real life are still very far from reality due to difficulties to match foundry lines. Traditional dynamic random-access memory (DRAM) is still the dominant memory device in IC.[6,8] The main volatile memory is DRAM, with a short programming time on the order of 10 ns and a retention time as short as 64 ms. Here, we propose a simpler memory transistor with simpler processing steps.[9] The memory transistor, based on flexible and transparent materials, is proposed for medical applications, with the advantages of a fast programming time comparable to DRAM and much longer retention times. Such memory could be a potential alternative candidate to DRAM for information technology applications.

Meanwhile, numerous nanomaterials (such as nanotubes and 2D flexible materials) have been investigated for memory devices due to their lightweight and improved electrical properties.[9–15] In addition, they can be mass produced without high cost, similar to silicon, due to their amorphous properties. One of these amorphous oxide semiconductor (AOS) nanomaterials is In-Ga-Zn-O (IGZO). This is because with a scaling down requirement of modern IC, advanced nanomaterials have become more and more attractive. For instance, the semi-floating gate transistor would involve 2D AOS nanomaterials to introduce more of a junction tunneling effect to enhance memory properties.[9] Amorphous oxide semiconductors have been studied due to their attractive properties including transparency, flexibility, and moderate mobility. Further, the artificial synaptic devices based on AOS have been widely studied due to potential applications in AI, neurocomputing, and medicine. For example, representative artificial synaptic transmission behaviors are required to be obtained quantitatively in order to mimic clinical behaviors. In order to mimic transmission behaviors easily, an equation is proposed to facilitate related AI and medical studies. The objective of this study was to propose simplified memory designs with advanced nano materials. Here, our devices are the first artificial synaptic transistors based on a flexible polyvinyl alcohol (PVA) grid insulating layer.

Methods

As shown in Figure 1, the processing of such an updated memory structure could be similar to a transistor. The

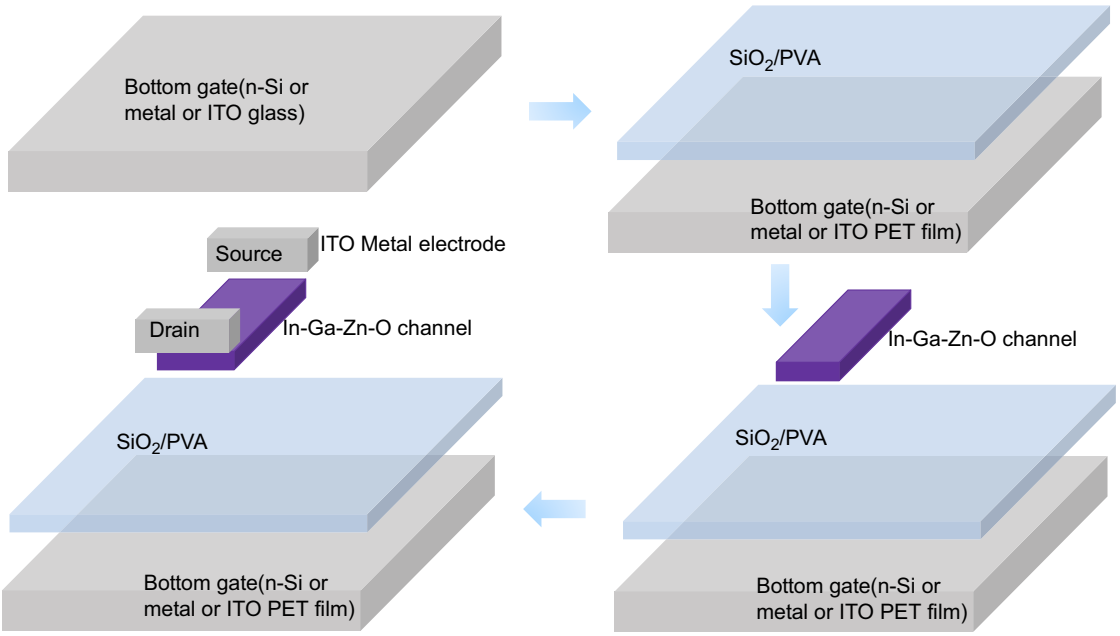

Figure 1 Schematic and process flow of the memory based on oxide nanomaterials.

preparation process of the samples with the bottom gate top contact structure is as follows. On one hand, the transistor has an n-type Si doping on the Si wafer as the bottom gate layer. The SiO_2 thickness was about 100 nm. PVA was then grown on the bottom gate layer as the dielectrics layer by spin coating. On the other hand, for the flexible transparent thin film transistors, PET was used as a flexible substrate with ITO on the top as the bottom gate. The gate insulation layer was prepared by PVA. A 10 wt% polyvinyl alcohol solution was prepared by dissolving PVA by magnetic stirring and heating, under atmospheric pressure and room temperature. Afterward, a PVA grid insulating layer was prepared by a spin coating method, first coating at 200 rpm for 3 s, then coating at 2,000 rpm for 20 s. The samples with coated PVA films were then heated at 900°C for 30 min. Different advanced transparent materials (such as PI) were also proposed to play a role as dielectrics, but PVA fits best here. Afterward, an n-type oxide semiconductor, indium gallium zinc oxide (IGZO), was deposited on the PVA as the channel layer. The 35 nm thick channel was formed by magnetron radio-frequency sputtering with designed masks and only the IGZO channels were deposited separately. Parameters of flow rate, sputtering time and pressure were 14 sccm, 5 min, and 0.5 Pa, respectively. The metal electrode layer for the drain and the source of the channel was deposited by electron beam evaporation and masks. The channel widths and lengths were 200 μm and 400 μm, respectively, with a thickness in the nanometer regime to maintain transparency and flexibility attractive for medical applications. The drain and source electrodes have a length and width as 150 μm and 1,000 μm, respectively.

Results

A top microscope view of the transparent memory transistor is shown in Figure 2. As shown in Figure 2, the top and bottom long transparent lines where the pins probe are the ITO drain and source electrodes, respectively. The transparent section between the drain and the source is the IGZO channel. Figure 2 also shows that the memory transistor is totally transparent and flexible.

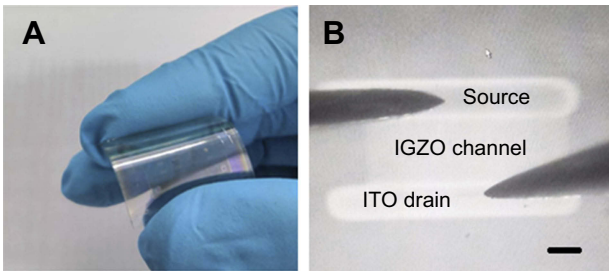

Figure 2 (**A**) A view of the transparent and flexible memory transistor. (**B**) Top view of the memory transistor with two pins probed on the source and drain electrodes. The channel width is 400 μm, and the length is 200 μm, scale bar=150 μm.

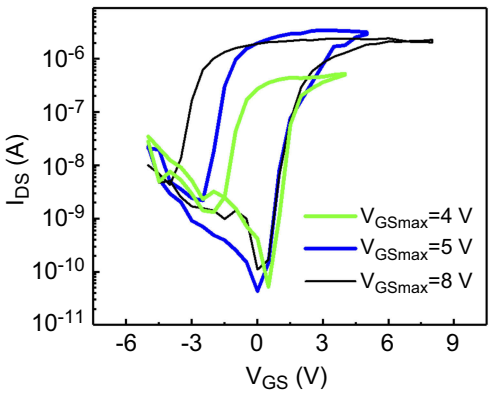

Figure 3 Transfer curves of a one memory transistor before and after programming at V_{DS} =1.5 V.

A typical memory curve is the transfer curve window of the memory transistor,[1,12] as shown in Figure 3. The hysteresis loop of the transfer curve is named the memory window. The memory window could be increased by the maximum gate voltage V_{GSmax}. It is shown here that a higher gate voltage V_{GS} could lead to a larger memory window. This is because of an enhanced programming effect. The window could be as large as over 4 V, which is a window large enough for memory function. The initial measurement curves could be repeated in all of the three measurement curves sweeping from a negative V_{GS} to positive V_{GS}, which suggests that the device characteristics show good repeatability. The general difference of the memory window is mainly generated by V_{GS} and is demonstrated on the left part of the memory window where V_{GS} sweeps back from a positive to a negative V_{GS}. It is shown that both the voltage difference range and the current difference range increase with a larger V_{GS}. The reason is that V_{GS} leads to a programming effect of the memory device so that a larger V_{GS} leads to an enhanced memory effect.

The programming is as follows. When V_{GS} is positive, the IGZO semiconductor channel is turned on, and there are a lot of mobile electrons along the channel. The electrons are attracted to the ITO drain and source electrodes and stored in the junction between ITO and IGZO. Such electron storage in the ITO/IGZO junction could repel electrons moving them toward the junction on the channel top surface side. This facilitates electron carriers to move towards the channel bottom side near the bottom gate to contribute to the channel

current. In this way, the channel current could be enhanced when the same V_{GS} is applied, due to the electron storage into the junction of the ITO/IGZO. When the same V_{GS} is applied, the channel is turned on more easily. When V_{GSmax} increases, the programming effect is enhanced so that the memory window is enlarged.

In addition, as shown in Figure 3, the drain current I_{DS} could be adjusted with V_{GSmax}. As a higher V_{GSmax} is applied, it could lead to a higher I_{DS} at the same V_{GS} when V_{GS} is swept back from positive to negative values. The current on/off contrast, which is also one of the memory properties, could be adjusted from 10^4 to 10^5 in the sample data presented here due to different V_{GSmas}. This suggests a multi-level charge storage application, and the value of the memory charge level could be adjusted. The on/off state contrast and hence the retention time after programming could be adjusted by the voltage bias, according to Figure 3. This shows that the memory transistor has a potential application to replace DRAM also. With proper adjustment, such as proper programming conditions and semiconductor materials, the memory current on/off contrast and thus the memory retention time correlating to such contrast could be controlled.

Discussion

The carrier injection into the junction between the layers is the key mechanism behind the memory properties. While there are IGZO and ITO nanomaterials deposited in sequence, a junction is formed between IGZO and ITO. As shown in Figure 3, when V_{GS} <0, the channel is turned off. When V_{GS} >0, I_{DS} >0, ie, the semiconductor channel is turned on. In this case, the transistor using such processing is a nMOS (n-type metal oxide semiconductor) transistor. For a typical nMOS transistor, the majority of carriers are electrons. Therefore, the mobile carriers in the channel are electrons. Figure 4 explains the programming process of such a transparent memory transistor. As shown in Figure 4, when a gate voltage V_{GS} is applied on the Si bottom gate, a drain voltage V_{DS} is applied on the drain, there is a vertical electrical field between the semiconductor junction (ITO-IGZO) layers. When V_{GS} >0 and V_{DS} >0, the electrons are injected into the junction between the ITO electrodes and the channel, and vice versa when V_{GS} <0 and V_{DS} >0. In this way, the programming process in the memory device can be implemented.

For ITO-IGZO junctions, it has been previously shown to be one of the fastest speeds reported for memory devices.[12] Even with such a short programming time on the order of 10 ns, an obvious current on/off state contrast could be observed

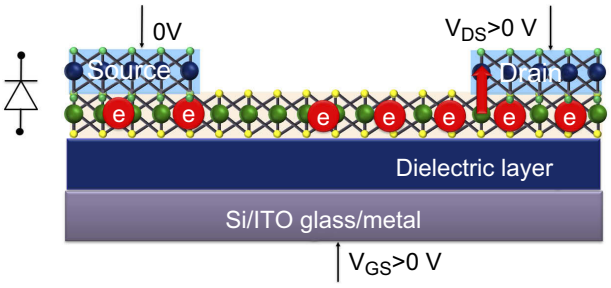

Figure 4 Cross section schematic of the one transistor memory programming during IV measurements.

after the programming. The programming time on the order of 10 ns is among the fastest programming times.[1,12] This is limited by the minimum value of pulse generators (three generators are needed for the pulse voltage for programming applied on the drain control gate and top gate, respectively) and is on the same order of DRAM (10 ns).

In addition, our configuration and one-transistor memory structure could also be used as synapse devices.[13–15] Synapse characteristics (such as signal processing functions) named excitatory postsynaptic currents (EPSC) useful for both memory loss and memory retention loss were investigated in our structure.[13] As shown in Figure 5A, EPSC reaches a peak value I_0 and decreases gradually, which is similar to that in a biological excitatory synapse. A V_G spike on the gate generates transient ionic fluxes in the semiconductor layer and an excitatory postsynaptic current EPSC in the transistor drain could be measured. For the 2-terminal measurement, which is a typical synaptic measurement, we can measure EPSC from the drain by applying a spike V_G on the gate.[15] For 3-terminal measurements, we did the same measurement as with a 2-terminal one by adding the source voltage as 0 V.[13] As shown in Figure 3A, power consumption was 5 pJ, which is on the same order of the dissipation aim for a neuromorphic system application.[16] Here, the width of our sample is 10 μm. Given a smaller device, power dissipation could be reduced.

As shown in Figure 5A, the decay of EPSC in the 3-terminal samples is generally larger than that in 2-terminal samples. They both can be described by a stretched exponential function:[13]

$$I = (I_0 - I_\infty)\exp\left[-\left(\frac{t - t_0}{\tau}\right)^{\beta}\right] + I_\infty \qquad (1)$$

where τ is the retention time, t_0 is the time when the presynaptic spike finishes, prefactor I_0 is the triggered EPSC at the end of the presynaptic spike, β is the stretch index

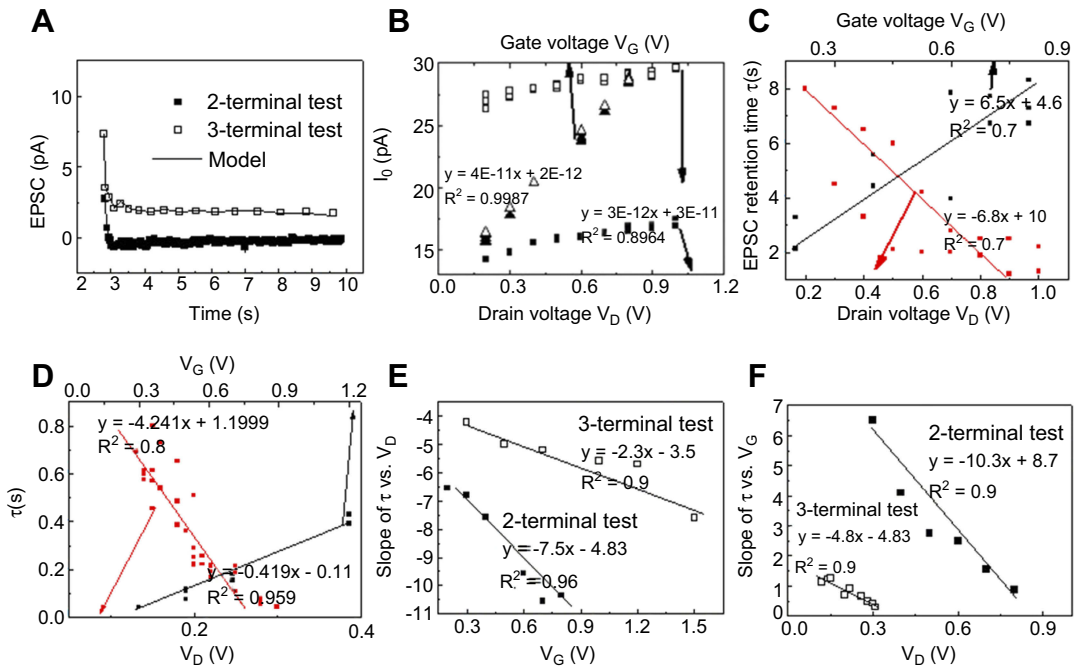

Figure 5 EPSC I triggered by a presynaptic spike on the bottom gate with 2- and 3-terminal measurements. (**A**) Eq. (1) fits well with the measurement of both 2- (with a spike on the gate, amplitude as V_G, and DC drain voltage V_D) and 3-terminal (with a spike on the gate, V_D and source voltage V_S=0) EPSC. (**B**) Amplitude in Eq. (1) increases with both V_G and V_D for 2-terminal measurements. (**C**) EPSC retention time τ vs voltage for 2-terminal measurements. (**D**) τ vs voltage for 3-terminal measurements; arrows represent the corresponding y-axis. (**E**) Dependence of τ-V_D slope on V_G. (**F**) Dependence of τ-V_G slope on V_D.

ranging between 0 and 1, and I_∞ is the final current of the EPSC test. As shown in the fittings of Figure 5B–F, I_0 and τ show a linear dependence on both gate spike amplitude V_G and drain voltage V_D, which means that different shapes of EPSC could be obtained easily by adjusting V_G and V_D.

With these voltage dependence findings, we can easily realize desired synaptic behaviors without changing materials or spike cycles. Figure 5B shows that I_0 increases with increasing V_D and V_G, which could be found in 2- and 3-terminal measurements. Figure 5C and D show that the τ of EPSC was reduced by increasing V_D, but increases when V_G increases. Figure 5E and F show that the τ-V_G slope is impacted by the V_D and τ-V_D slope by V_G. Thus, Eq. (1) can be updated as:

$$I_0 = x \cdot V_G \cdot I_{01} + y \cdot V_D \cdot I_{02} + z \quad (2)$$

$$\tau = a \cdot V_G \cdot \tau_0 - b \cdot V_D \cdot \tau_0 + c \quad (3)$$

$$a = -d \cdot V_D \quad (4)$$

$$c = -e \cdot V_G \quad (5)$$

where a, b, c, d, e, x, y, and z are constants.

With the updated models, complex synaptic device behaviors with different I_0 and τ would be emulated easily, including EPSC, and memory loss behaviors including both STM (short term memory) and LTM (long term memory).[5,18] The model is based on measurements performed on over 10 samples, and each finding from the trend was repeatable. The quantitative models can give a guideline of how to adjust V_G and V_D to obtain different synaptic behaviors in a certain voltage range, although the constants need to be adjusted for different processing and devices.

Conclusion

The first transparent and flexible one-transistor design for memory without an additional process to a typical transistor has been proposed and implemented here. It was fabricated using oxide nanomaterials with nanometer thickness attractive for numerous medical applications, such as wearable (or even implantable) sensors. Its window is as large as 4 V with a high current on/off state contrast before and after programming as large as 10^5. The mechanism of this compact memory is attributed to a junction between the transistor channel and electrode. This memory is likely to be used as alternative memory with quasi-non-volatile memory as an alternative for DRAM in information technology, with its simple design and adjustable electrical properties such as bias-dependent current on/off state contrast and window. This memory structure shows artificial synaptic behaviors and could be used in

neuromorphics for artificial intelligence applications. This first transparent and flexible one-transistor design for memory without an additional process to a typical transistor is based on PVA, and could be a potential candidate for electronic skin, portable electronics, artificial intelligence, and sensor applications.

Acknowledgments

This work was supported by the National Science and Technology Major Project of the Ministry of Science and Technology of China (2017YFB03031001), the National Natural Science Foundation of China (Grant No. 61574147), Zhejiang Provincial Natural Science Foundation for Distinguished Young Scholar (Grant No. LR17F040002), Instrument Developing Project of the Chinese Academy of Sciences (Grant No. YJKYYQ20180021), and the Project of the National Natural Science Foundation for Major Research Projects (91648109).

Author contributions

All authors contributed to data analysis, drafting and revising the article, gave final approval of the version to be published, and agree to be accountable for all aspects of the work.

Disclosure

The authors report no conflicts of interest in this work.

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